TUG 2012

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MULTIPLE TPS REHOST FROM GENRAD 2235 TO S9100

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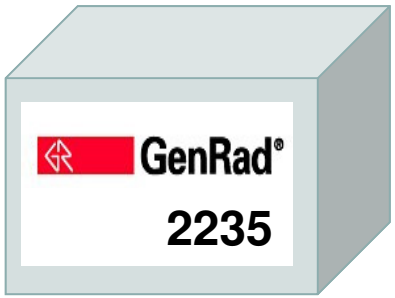
WHAT IS THE PROBLEM?

- **Obsolete Equipment**
  - Over 30 years old
  - Difficult to Maintain
- **Continued Coverage Required**
  - UUTs used in critical plant safety control

SOLUTION

1. NEW TESTER
2. NEW ITA
3. REHOSTED TPS

UPGRADE TO S9100



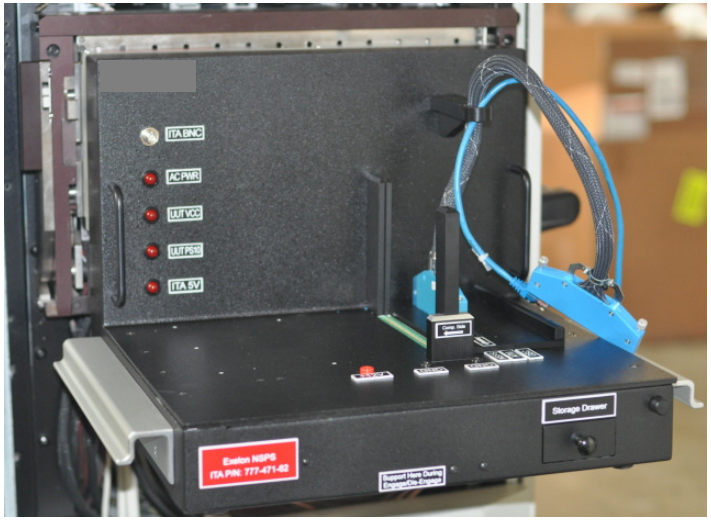
Digital only
120 channels

Spectrum 9100

Single bay S9100 tester with two Di-Series cards – 128 channels.

NEW ITA

Old ITA



New ITA

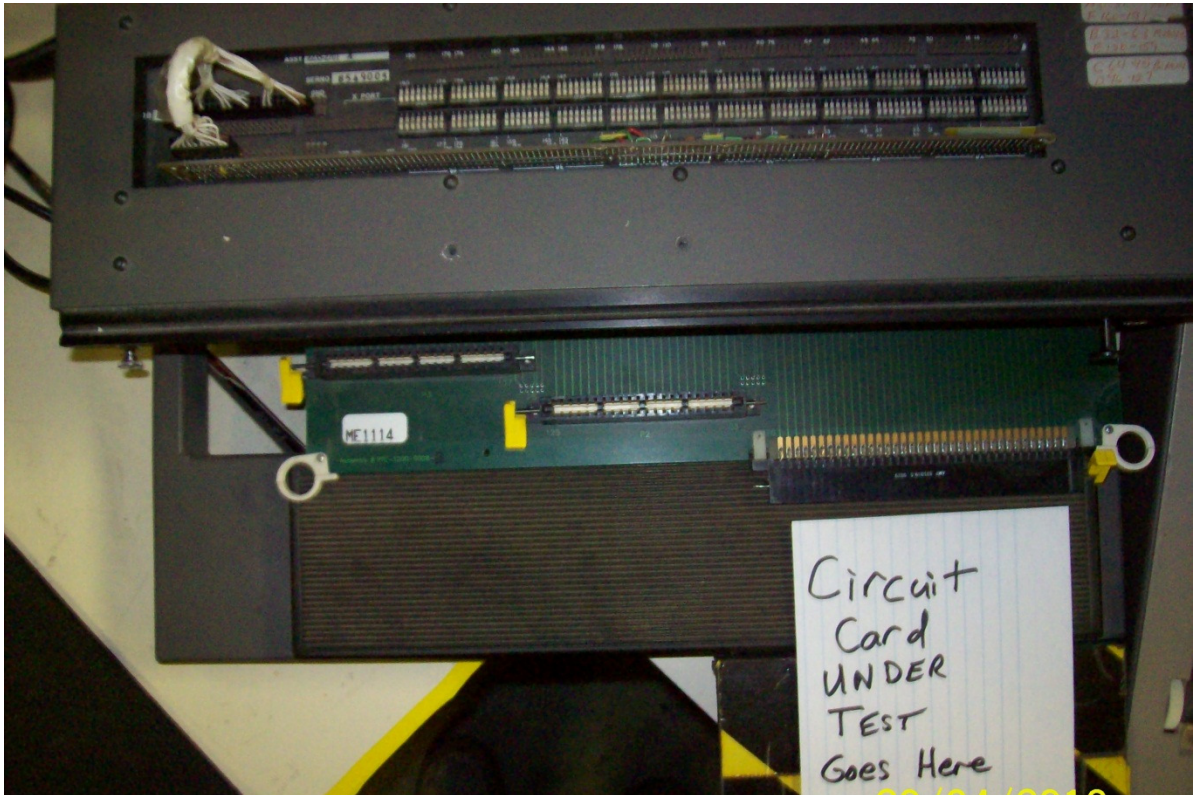
ITA DESIGN – "Forensics"

- Reverse Engineering "Forensics"

- Hand-drawn personality cards – not 100% accurate

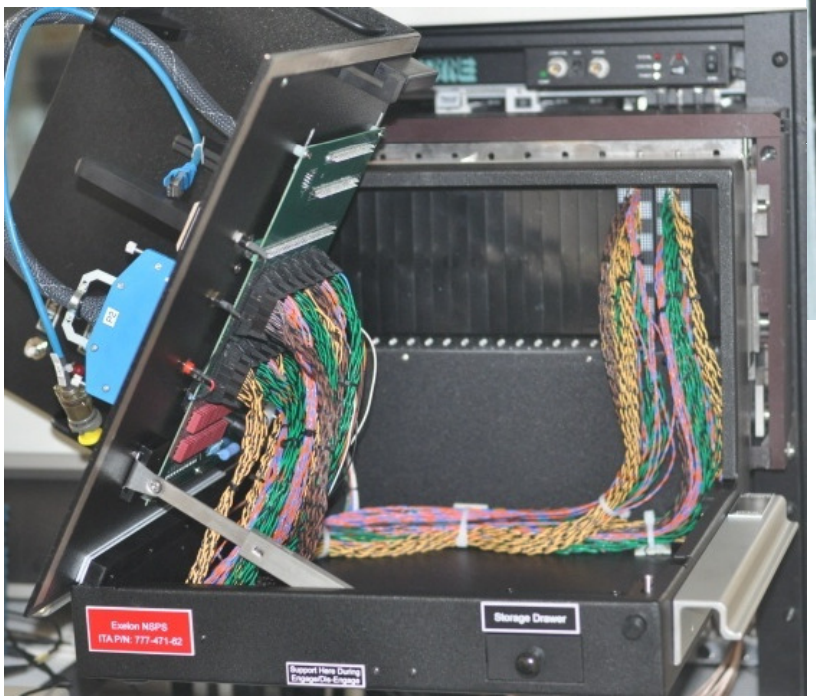
- Photo of hardware to reverse engineer

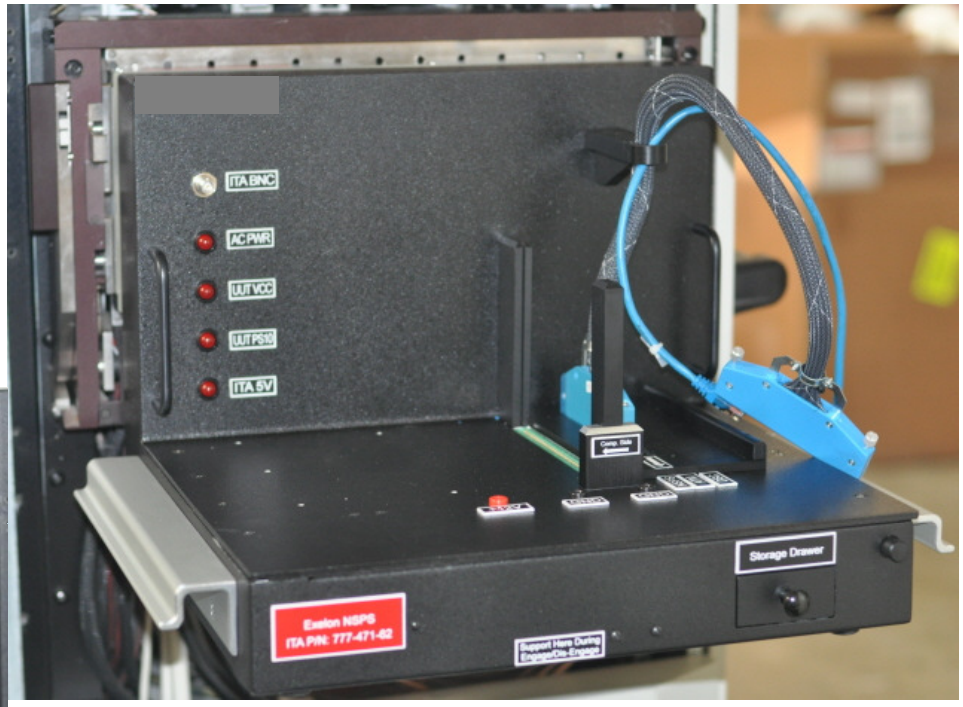
- No GenRad 2235 tester hardware reference document



NEW ITA – "ALL IN ONE"

Multiple UUT insertion positions + cables



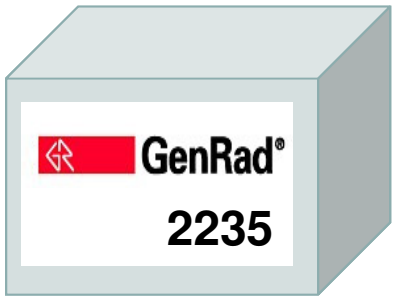


PCB based personality card
- Incorporate signal switching
- Eliminate wiring errors
- Add accessibility for debug

TPS REHOST – "HARDEST PART"

- 47 Test Programs on 8 inch floppy
- Customer does not have all UUT design specification
- Customer has no in-house knowledge of existing GenRad tester or the TPS

TPS REHOST –"TRACEABILITY IS MUST"



Tester Architecture

Spectrum 9100

BASIC Programming language **C++**

- No time and resources to do-it-all-over; certification will take years
- No tools such as TPS Converter Studio for L200 to provide traceability

TPS REHOST

1. TPS TRANSLATOR
2. EMULATE GENRAD BEHAVIOR
3. ADD NEW TESTS

WHAT DOES THE TRANSLATOR DO?

Original TPS

10050 IH 29,30,22,34,5; X

Translator

Main.cpp

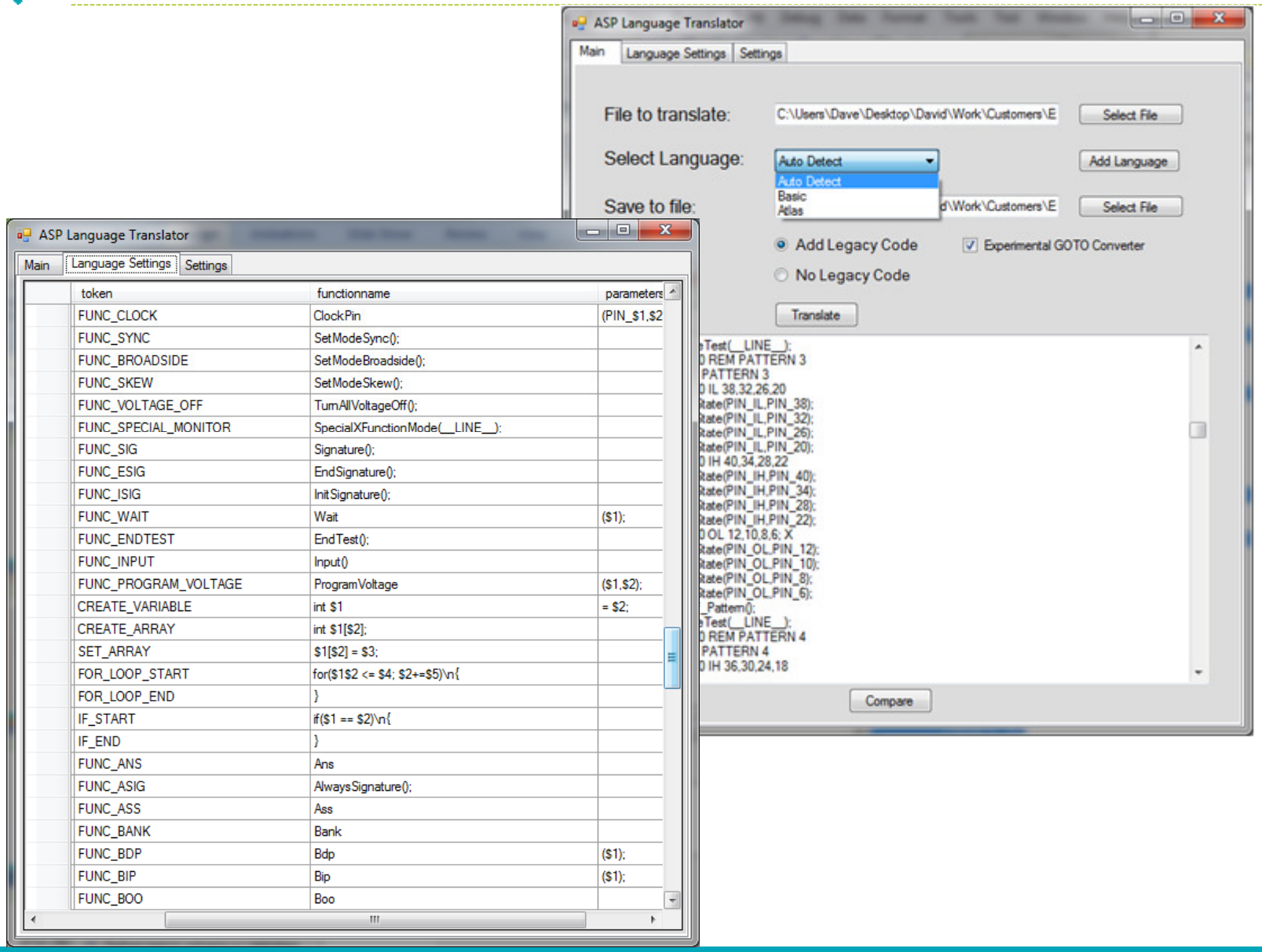
```
//10050 IH 29,30,22,34,5; X
SetPinState(PIN_IH,PIN_29);
SetPinState(PIN_IH,PIN_30);
SetPinState(PIN_IH,PIN_22);
SetPinState(PIN_IH,PIN_34);
SetPinState(PIN_IH,PIN_5);
End_Of_Pattern();
XFunction(__LINE__);
```

Source code level traceability

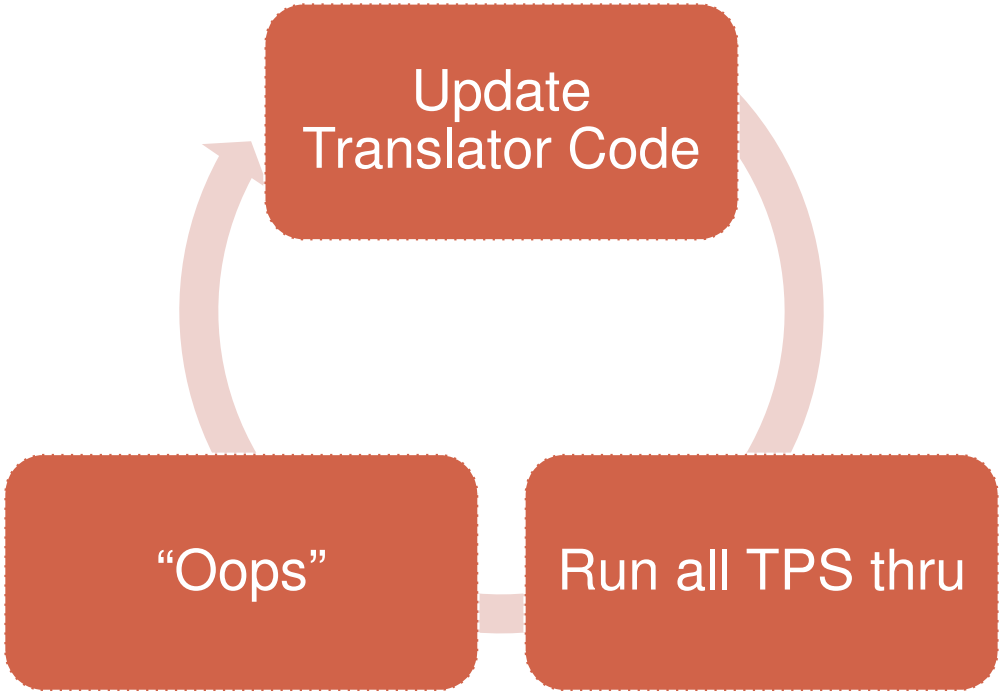
HOW DID WE IMPLEMENT THE TRANSLATOR?

- **Use GNU Tools**
- **Flex**
  - A fast lexical analyzer generator
  - It is a GNU tool for generating programs that perform pattern-matching on text
  - http://flex.sourceforge.net/
- **Bison**
  - General-purpose parser generator
  - http://www.gnu.org/software/bison/

WHAT DOES IT LOOK LIKE?



HOW TO MAKE IT PERFECT?



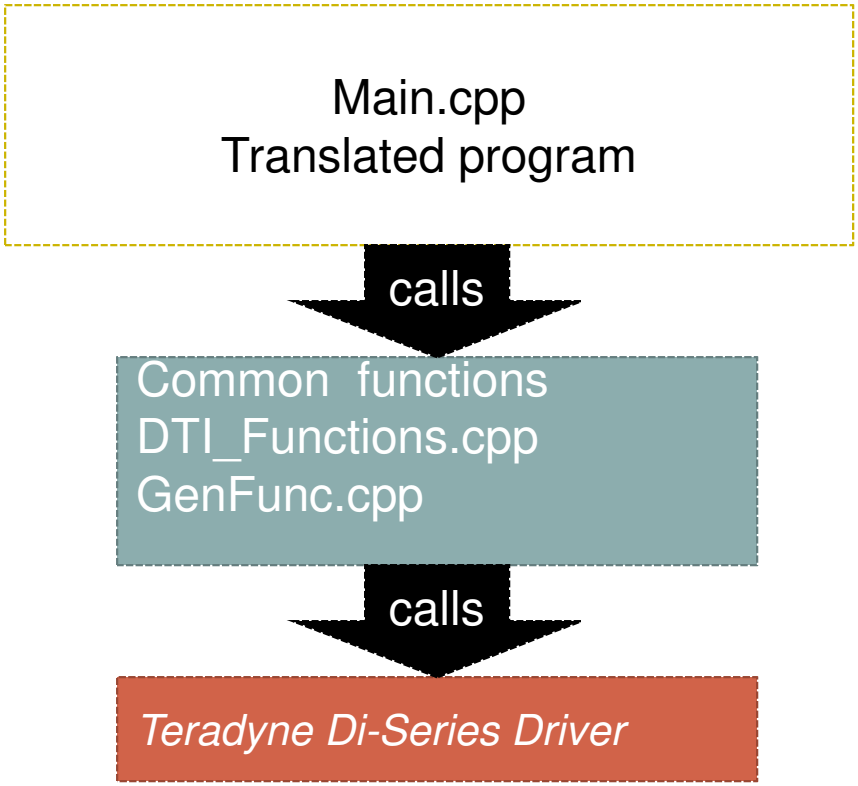
WHY DID WE HAVE SO MANY "OOPS"?

- No 8-inch floppy drive, so rehosted from paper copy
  - TPS were printed on paper with dot matrix printer … years ago
- TPS code on printout was scanned and ran thru "OCR" (optical character recognition)
- OCR is not perfect!

- Human inspectors – multiple of them are required! Multiple passes too!

47 Test Programs on 8 inch floppy

EMULATE GENRAD BEHAVIOR



Shared Emulation Library

- Used by all translated TPS
- Emulate GenRad test behavior

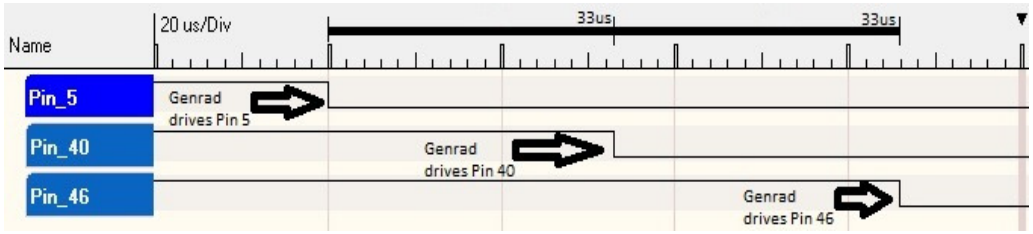
EMULATE GENRAD BEHAVIOR

- Timing Differences
- Execution Differences
- Power Differences

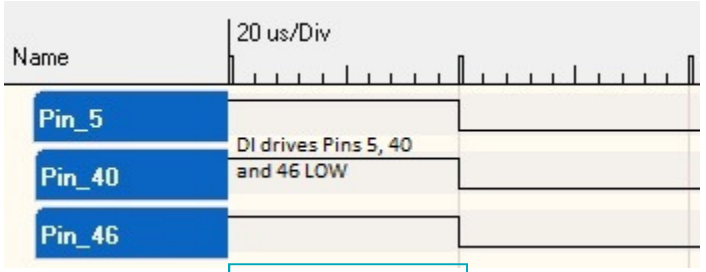
TIMING DIFFERENCES

- GenRad
  - Interpretive Language: commands executed as they are read
  - Timing between test states is the time it takes the CPU to read, parse and then execute a test command
  - Apply digital stimulus one pin at a time with a ~32us gap before it can drive the next input pin
- Di –Series
  - Precise, repeatable digital stimulus and measurements independent of PC
  - Drive all stimulus pins in the same state all at the same time
  - **Dynamic Mode; Set TSET period to 40us**

Example: IL 5,40,46



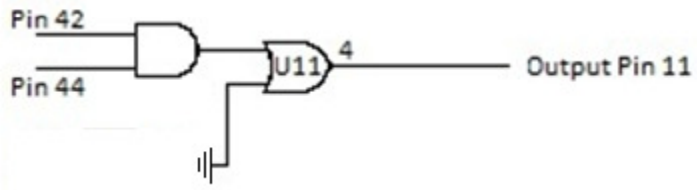
GenRad

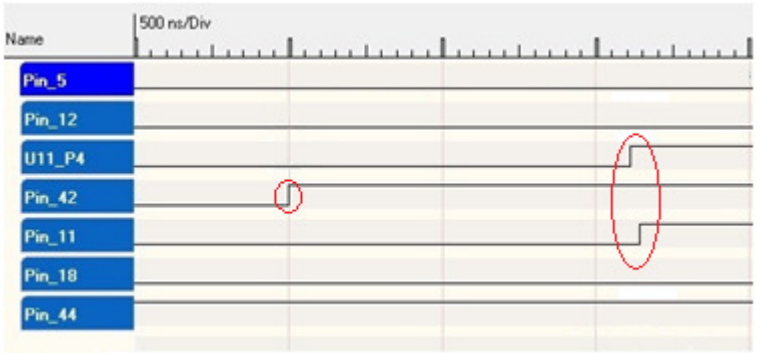


Di-Series

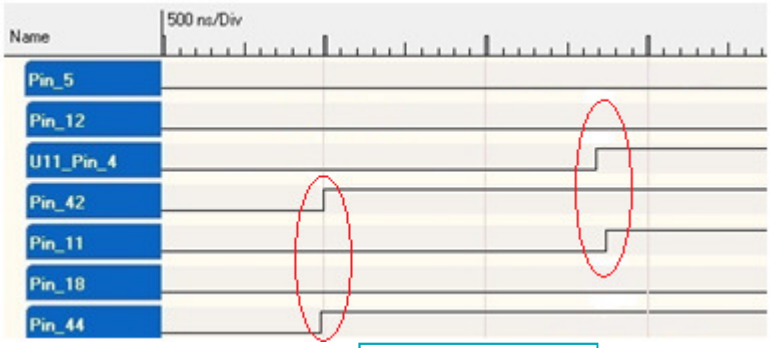
TIMING DIFFERENCES – DIGITAL ANALYSIS

- Digital circuit
  - The logic circuits outputs are dependent on their input(s) and respond “immediately” when the input changes
  - Both testers use the same 10us timing to test the output giving the logic circuits ample time to change their output
- Verified with several typical logic test setup





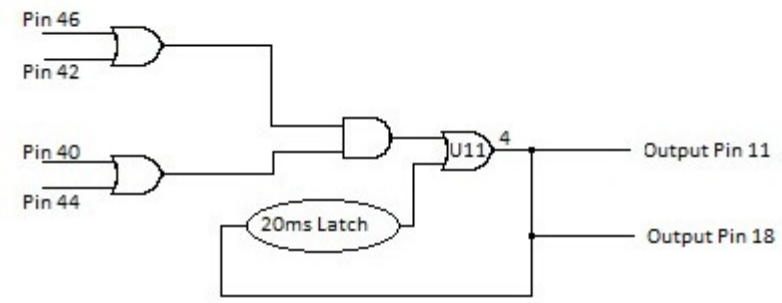
GenRad



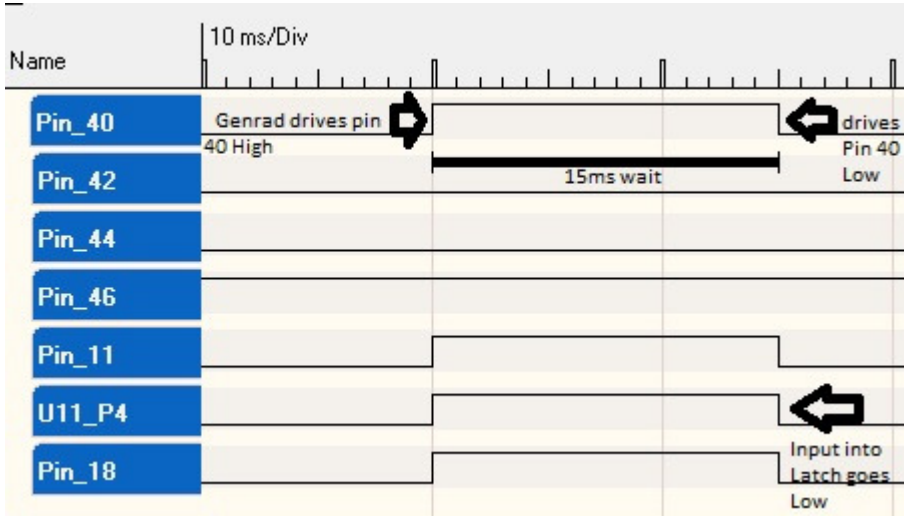
Di-Series

TIMING DIFFERENCES – ANALOG ANALYSIS

- Analog circuit
  - Typical analog circuits in this project use logic circuits to directly control the analog circuit's input
  - Allows each tester to use digital stimulus to control the analog circuits with precise timing



Di-Series Card results showing
- pin 40 driven high
- waiting 15ms
- driving pin 40 low
- causing the input into the 20ms latch to go low



TIMING DIFFERENCES – CLOCK IS SPECIAL

- Genrad digital commands execute in 40 microseconds
- CLOCK statement toggles at its own timing
  - CLOCK timing not documented
  - Verified GenRad's Clock is a fixed pattern 8us high and 8 us low

Resolution

- Add second timing set on Di-Series to be assigned to clock pins
- TSET 0 is set to 40us period while TSET 1 is set to 8us. Whenever the setClock() function is called the TSET is changed from 0 to 1

EXECUTION DIFFERENCES

- Di-Series
  - Load up the patterns and then execute dynamic burst
- GenRad - executed statement by statement
  - Patterns are not preloaded
  - Decision making in the middle of a pattern is part of timing
  - The X statement is part of the timing

- **Resolution**
  - Insert patterns to account for GenRad decision making delay
  - At X statement, insert extra pattern

TESTER POWER DIFFERENCES

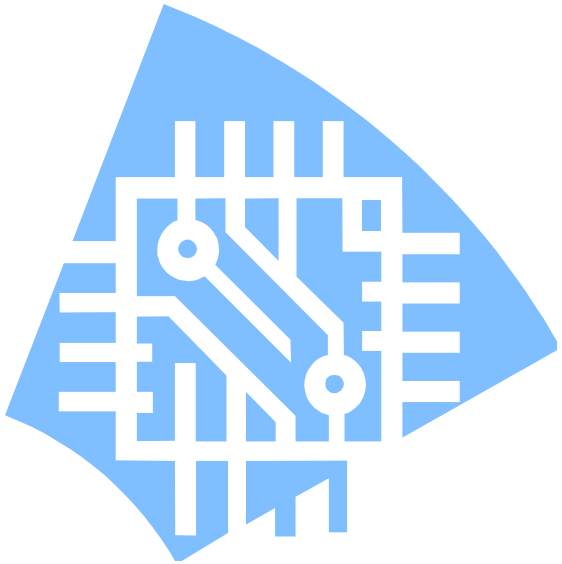
- GenRad
  - Power supply had a hardcoded/hardware current limit of 20mA
  - Tester can drive 500mA per channel
  - Test was designed to turned on the digital channels to provide extra power when the board needed it
- S9100 Tester
  - Power supplies current limit can be programmed
  - Di-Series drives 80mA

Resolution

- Removed code using digital channel to assist power-up board
- Set the power supply current limit based on the UUT design specification

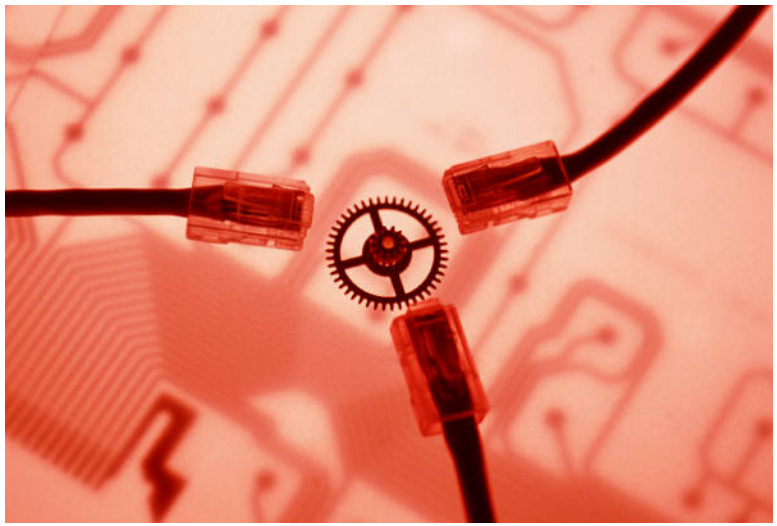
NEW TEST CAPABILITIES

- Added Additional tests
  - Shorts and Opens Tests
  - Current Limiting Tests
  - Voltage Measurement
- Improved Test Diagnostics
  - Detailed Failure Information
  - Improved Component Failure Information



INTEGRATION - PUTTING IT ALL TOGETHER

- Pieces to Integration
  - Translated Test Program Code
  - Test Studio TPS Project
  - Added Tests
- Test with Simulation
  - Test the lower level implementation
  - Test Drivers



TPS TRANSLATED

INTEGRATION & VALIDATION

WELCOME TO ILLINOIS

ACCEPTANCE TASKS

- ITA design review
- Translator validation
- Each TPS source code compare / Validation
  - Don't take the engineer(s)' word for it
- ITA self test
- Passing known good boards
- Fault insertion and detection
  - Prove it can catch faults
  - Demonstrates failure logging
- Hands-on customer training

VALIDATION CHALLENGES

- Known Good Boards are Hard to Come By
- Timing Matters
- Test Results Not Correlating Between Testers
- UUT Configured Improperly
- Fault Inject Issues

KNOWN GOOD BOARD – HARD TO COME BY

- Some boards were at unknown states
- Some boards required calibration
- Some boards identified incorrectly (labeled wrong)
- Some boards with components out of spec

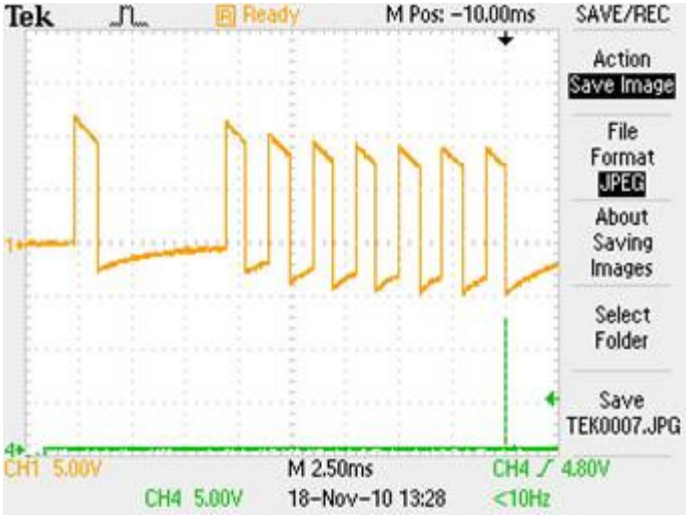
- Capacitor out of tolerance
  - Supposed to be 0.47uF, but on the board was a 0.61uF
  - Caused timing problem

TIMING DOES MATTER!

- Spectrum test execution is too fast for the UUT to keep up
- GenRad system is slow enough not to see this problem
- UUT design specified the requirement of minimum settling time between test bursts

Resolution

- Add a delay of 30ms delay to comply with UUT specification of 3% max duty cycle on the line

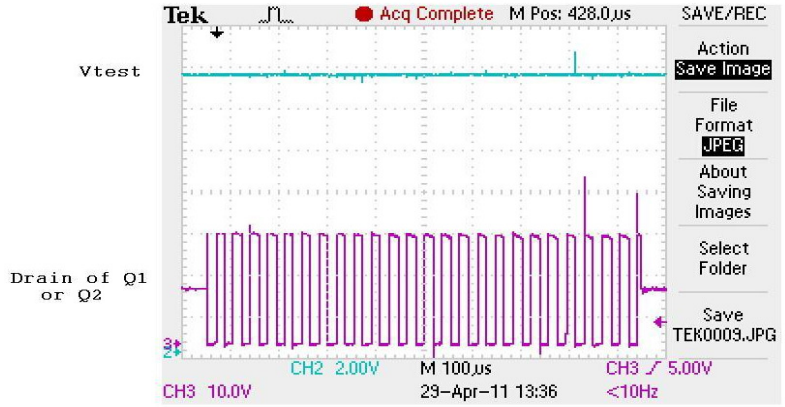


TEST RESULTS NOT CORRELATING BETWEEN TESTERS

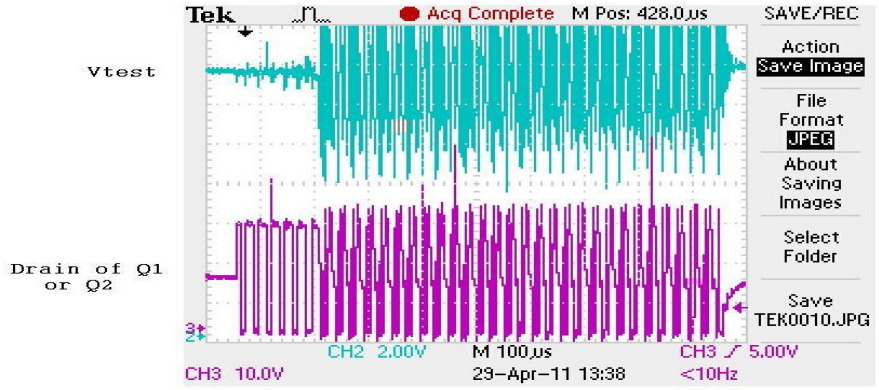
- One variant of UUT failed on Spectrum, but passed on GenRad
- Power input fluctuates on the Failed UUT
- UUT Drawing Power from DI Cards
- Related to Power Differences Mentioned Earlier
- Drive Monitor Pin Failure Only

Resolution

- Change Drive Monitor to Drive Only on the failed pin



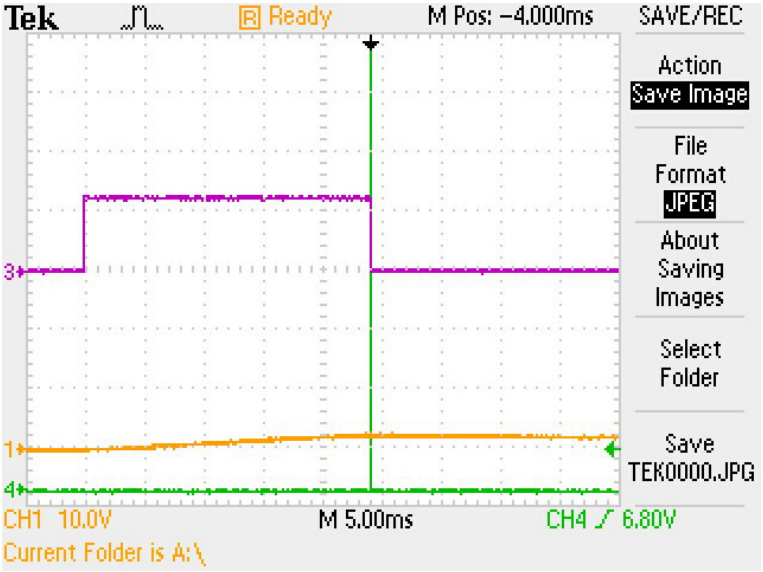
A working variant with clean output

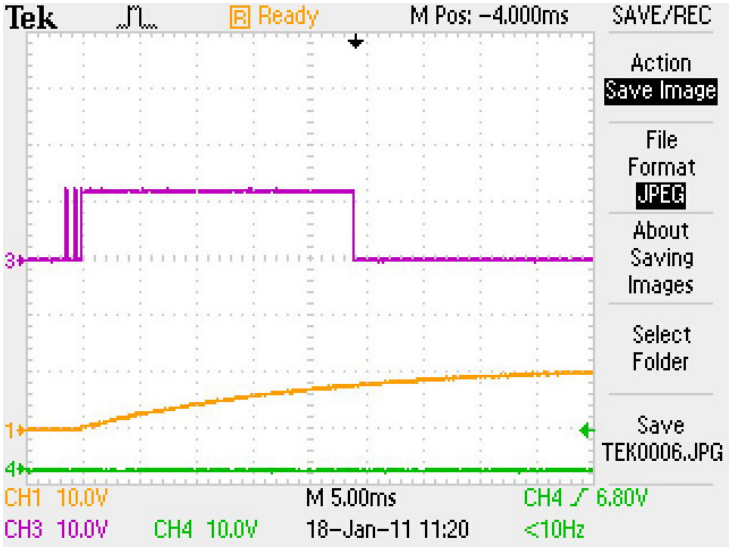


A failed variant with transformers' cores being saturated

UUT BOARD NOT CONFIGURED PROPERLY

- Compared similar RC circuit between failed UUT and a passing UUT; computed the capacitive value
- Concluded the adjustable resistors on the failed UUT were not set to the correct values and need to be adjusted to values similar to the passing UUT's resistor values





DEFAULT PIN STATE MATTERS

- Default state of channels matters
  - On the GenRad tester, the tri-stated pins drift HI
  - On the DI, the tri-stated pins were pulled to VCOM, in this case were set to LO

Resolution

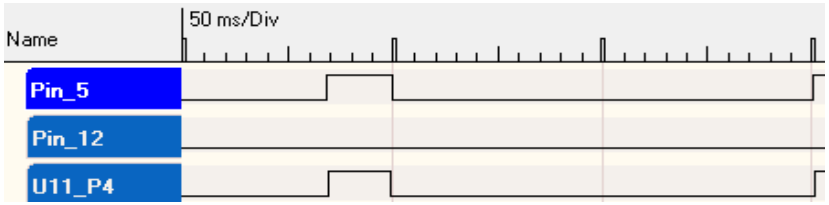
- Match the GenRad behavior and fail the same pin under the fault injection condition
  - Modified the tester initial setup to ensure the proper pin is pulled up to HI when it is not driven
  - This modification done in the Shared Emulation Library
  - No re-translation required

BOARD POWER OFF – BOARD STILL RUNNING!?

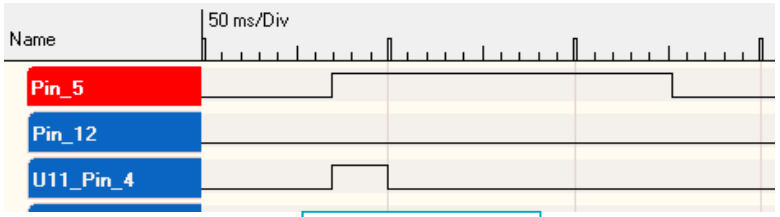
- Board power off but charged by capacitors
- GenRad does not meet board specification
- Complying caused pass when it should fail

Resolution

- SOF test will catch the missing fuse before executing functional test
- White paper to document the difference
- Leave Spectrum test as it



GenRad



Di-Series

RECAP

- The problem
- The solution
- Implementation
- Debug and Validation
- Lessons Learned

WHAT HAVE WE LEARNED?

- TPS rehost means “Matching” the old tester, for better or for worse
- We have to prove the tests are equivalent for both systems
- Emulating lower performance hardware is harder than you think
- White papers! A lot of them!

“The Customer [Tester] is Always Right!”

HOW DO WE THINK ABOUT OUR APPROACH?

- TPS translator is an adaptive learning process
  - Existing GNU tools make this easier
  - Development takes longer than expected because of continuous improvement
- TPS translator + Tester Emulation is efficient for multiple TPS Rehost
  - Provided traceability
  - Provided consistency across all TPS
  - Provided easy code change
- TPS translator can't replace people (yet!)
  - There are always special conditions
  - Hands-on tester characterization required

QUESTIONS?

THANK YOU

ENCORE - BONUS SLIDE

TIMEDLY2 Failure 3a - Pin 70 GND

(X)	PIN_INTLK1 (remove)	PIN_INTLK2 (remove)	PIN_69 (remove)	PIN_CARDSE (remove)	PIN_DATAOU (remove)	PIN_DATAIN (remove)	PIN_ECHO (remove)	PIN_TESTPL (remove)	PIN_A0 (remove)	PIN_64 (remove)	PIN_SELACK (remove)	PIN_62 (remove)	PIN_CLOCK (remove)	PIN_COMPAR (remove)	PIN_A1 (remove)	PIN_58 (remove)	PIN_A2 (remove)
0	ML	IOX	IOX	MH	IOX	MH	IOX	MH	MH	IOX	IOX	IOX	MH	ML	MH	IOX	MH
1	ML	OL	IOX	MH	IOX	MH	IOX	MH	MH	IOX	IOX	IOX	MH	ML	MH	IOX	MH
2	ML	IOX	IOX	MH	IOX	MH	IOX	MH	MH	IOX	IOX	IOX	MH	ML	MH	IOX	MH
3	ML	IOX	IOX	ML	IOX	ML	IOX	ML	ML	IOX	IOX	IOX	ML	MH	ML	IOX	ML
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