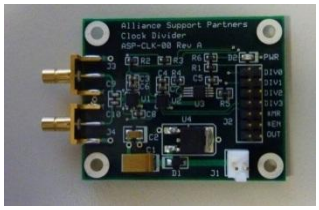
Alliance Support Partners, Inc.

ASP-CLK-00
2.5GHz Clock Divider

Revision: 1.0, October 28, 2011, Alliance Support Partners, Inc.

Product Overview

The ASP-CLK-00 Clock Divider is designed to divide high frequency signals, up to 2.5GHz, from 4 to 256 times. It will accept single ended (Unbalanced) or differential (Balanced) signals with amplitudes as little as 100mV rms.



The clock division is controlled by 4 shunt jumpers. The circuit can be disabled and the divide by counter reset with 2 control signals. The on board regulator will accept voltages from 4.85 to 15.0V. The output is capable of driving 700mV Peak to Peak into 50 Ohms.

Hardware Specifications

Model part number: ASP-CLK-00 rev A

Input frequency: 10 MHz – 2.5 GHz

Input impedance: 50 Ohm

Input Voltage: 100mv RMS (280mv PK – PK) to 1.16v RMS (3.3v PK – PK)

Output Impedance: 50 Ohm

Output Voltage: 700mv PK–PK (Into 50 OHMS) or 1.4v PK-PK (Into IM)

Power supply voltage: 4.85 – 15.0 V

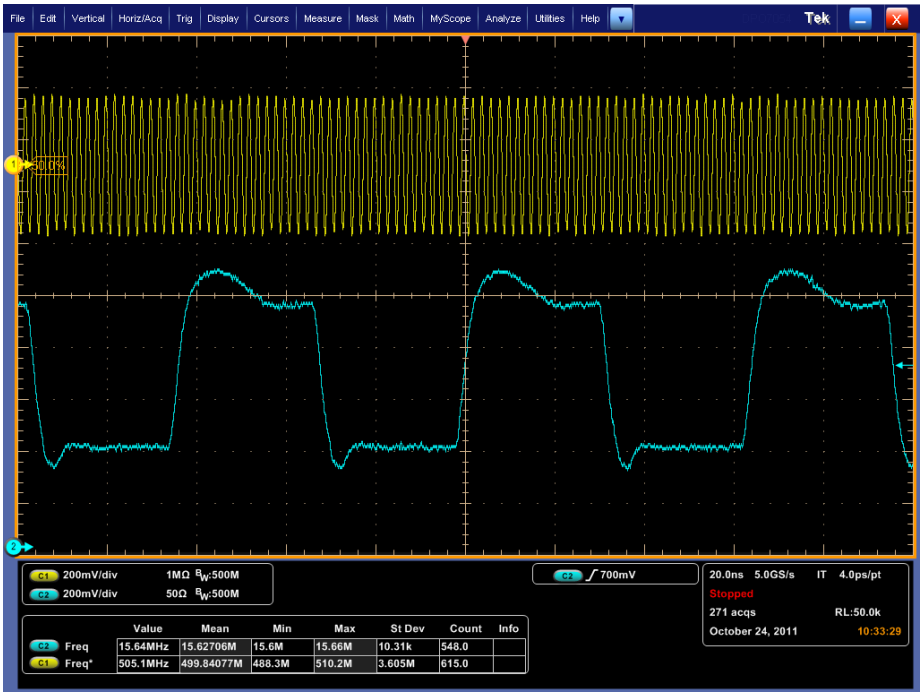
Power supply current: 110 mA

Clock divider divisions: ÷4, ÷8, ÷16, ÷32, ÷64, ÷128, ÷256

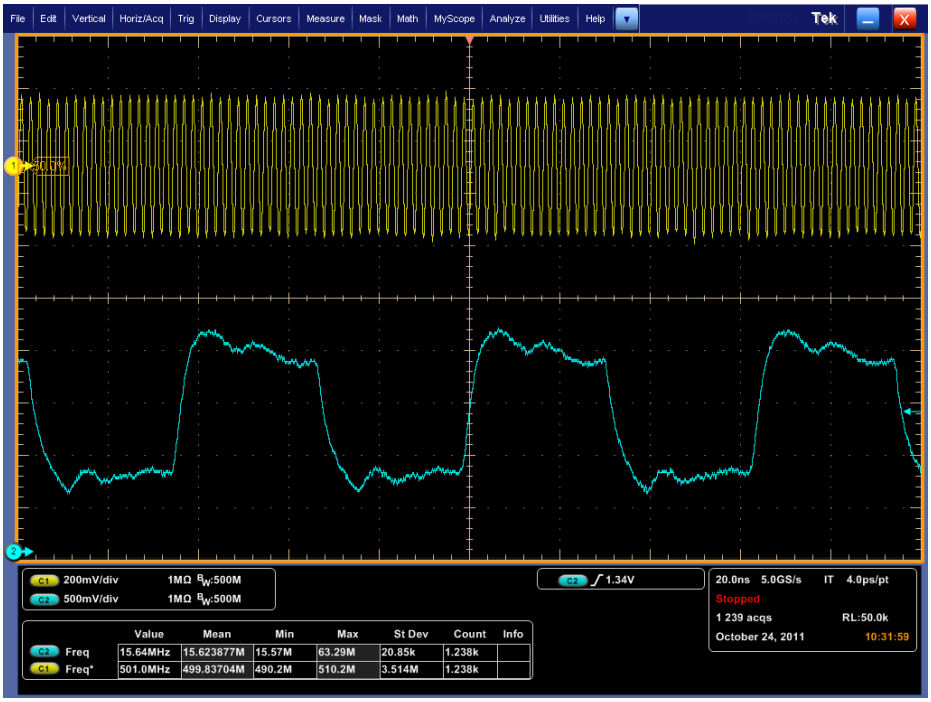
Physical dimension: 2” x 1.6” (5.08 cm x 4.06 cm)

Example Waveforms

Channel 1 = 500 MHz clock Channel 2 = ÷32 output into 50 Ohms.



Channel 1 = 500 MHz clock Channel 2 = ÷32 output into 1M.



Channel 1 = 50 MHz clock 100mv RMS Channel 2 = ÷4 output into 50 Ohms.